

REMARKS

The Examiner has rejected claims 1-9, 16-19 and 21 under 35 U.S.C. § 102(b) as being anticipated by Rotondaro et al. U.S. Patent Application Publication No. 2003/0109106. Claims 1-4, 6, 10-14 and 16 are rejected under § 102(e) as being anticipated by Bease et al. U.S. Patent Application Publication No. 2004/0129674. Claims 1-6, 8, 10 and 15 are rejected under § 102(e) as being anticipated by Egger et al. U.S. Patent Application Publication No. 2004/105213. Claim 20 is rejected under § 103(a) as being unpatentable over Rotondaro et al. or Bease et al. and further in view of Egger et al. The following remarks are respectfully submitted.

Independent claims 1 and 17 have been amended to specify that the thick high-k layer is deposited to a thickness so as to be continuous across its entire surface, and the thinning step reduces the thickness across the entire surface of the high-k layer such that the high-k layer is thin and continuous across its entire surface. Thereafter, a gate electrode is deposited on the thinned-down high-k layer.

Rotondaro et al. do not teach or suggest the claims as amended herein. Rotondaro et al. deposits a polysilicon layer 207 on the as-deposited high-k layer 205 to mask a portion thereof, and thereafter, only the un-masked, exposed regions of the high-k layer 205 are removed, by a two step process that first removes the bulk and then removes the remainder. Rotondaro et al. are disclosing a patterning process wherein the partial removal of the thickness of the high-k layer is only for an exposed portion of the high-k layer, i.e., it is not thinned across the entire surface of the high-k layer, and the thinning step is part of a complete etch-removal process of the high-k layer (where it is exposed) with the first thinning step using harsh chemicals to remove the bulk, which chemicals could damage the underlying layer, followed by a gentler etch to remove the remainder of the exposed high-k layer without damage to the underlying layer, which then becomes exposed upon completion of the etching. The masked portion of the high-k layer (under poly-Si layer 207) is neither thinned, nor removed, such that Rotondaro et al. do not teach or suggest the claimed method by which a thick, continuous high-k layer is thinned down across its

entire surface before depositing another layer on the thinned high-k layer.

Similarly, Bease et al. disclose a patterning process where a gate electrode 206 and mask layer 208 are applied to portions of a high-k layer 204, after which the other, exposed portions are removed in a two-step process in which the layer 204 is first modified or thinned with a harsher and potentially damaging chemical and/or process, followed by removal of the modified or remaining thinned layer by a gentler chemical and/or process. The portion of the high-k layer 204 under the gate electrode 206 is never modified or thinned, as shown clearly in Figs. 2a-2c, such that Bease et al. do not teach or suggest the claimed method by which a thick, continuous high-k layer is thinned down across its entire surface before depositing another layer on the thinned high-k layer.

Egger et al. disclose a process for forming a CAP layer 7 to encapsulate an electrode structure 3 formed on a substrate 1. The electrode structure 3 forms a pattern having horizontal surfaces, vertical sidewalls 17, and low inclined surfaces (of shoulder 5) that do not receive the CAP layer conformally, i.e., the CAP layer deposits across the entire patterned surface but with a greater thickness on the horizontal and low inclined surfaces than on the vertical sidewalls 17, as shown in the FIG. 2. Thus, the thinning step selectively removes thickness from the horizontal portions 9, 11 and low inclined portions 13 of the CAP layer 7 to match the thickness of the portion on the sidewall 17. Eggar et al. are addressing the problem of non-conformality of a continuous layer on a patterned substrate, whereas the present invention is directed to the problem of discontinuity in a layer deposited on a non-patterned substrate. Moreover, there is no disclosure of depositing a gate electrode on the thinned layer. Rather, Egger et al. is disclosing a method of forming a packaging layer (CAP layer) of consistent thickness that encapsulates an electrode structure. The claimed invention recites that the high-k layer is thinned across its entire surface, and thereafter, a gate electrode is deposited on the thinned layer. This is neither taught nor suggested by Egger et al.

As set forth above, none of the three applied references anticipate nor render

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obvious the claimed invention, as amended herein. It is therefore respectfully requested that all rejections be withdrawn.

In view of the foregoing amendments to the claims and remarks given herein, Applicants respectfully believe this case is in condition for allowance and respectfully request allowance of the pending claims. If the Examiner believes any detailed language of the claims requires further discussion, the Examiner is respectfully asked to telephone the undersigned attorney so that the matter may be promptly resolved. The Examiner's prompt attention to this matter is appreciated.

Applicants are of the opinion that no additional claims fee is due as a result of this Amendment. Applicants are also of the opinion that a 2-month extension of time is due with this Amendment. Payment of all charges due for this filing is made on the attached Electronic Fee Sheet. If any additional charges or credits are necessary to complete this communication, please apply them to Deposit Account No. 23-3000.

Respectfully submitted,

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